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Applicant:	Howard E. Rhodes	Examiner: Long Pham	
Serial No.:	09/782,743	Group Art Unit: 2823	
Filed:	February 13, 2001	Docket: 303.592US1	
Title:	DUAL DOPED GATES		

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the office action mailed on May 28, 2002. Please amend the above-identified patent application as follows.

6/13 9/16/02 JWm

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to include the previously pending claims and the new claims provided below.

C1

45. (New) The method of claim 1, preparing the substrate comprises forming a PWELL in an *n*-type substrate.

B1

46. (New) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises forming one or more complementary metal-oxide semiconductor dual gate structures in the substrate using only one mask.

47. (New) The method of claim 2, wherein forming the sacrificial oxide layer on the semiconductor comprises growing a sacrificial oxide layer to a depth of a few microns.

48. (New) The method of claim 3, wherein forming the gate oxide layer on the semiconductor comprises forming the gate oxide layer having a thickness of between about five nanometers and about ten nanometers.